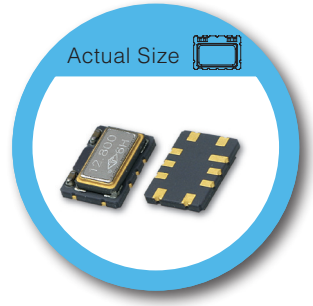
7.0 x 5.0 mm SMD Stratum 3 Voltage Controlled Temperature Compensated Crystal Oscillator – TS Type



RoHS Compliant Standard

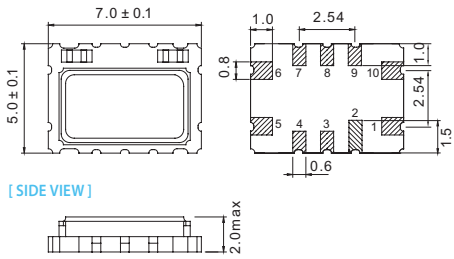
FEATURE

- Typical 7.0 x 5.0 x 1.85 mm ceramic SMD package.
- Stratum 3 (Overall ±4.6ppm including 20 years aging.)
- CMOS and Clipped Sine wave (without DC-cut capacitor) output optional.
- Packing: Tape & Reel 1000/3000pcs per Reel.

TYPICAL APPLICATION

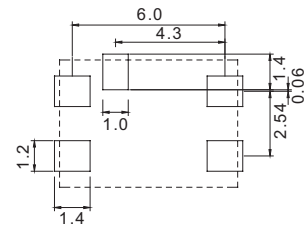
- Base Stations
- Stratum 3

DIMENSION (mm)



Pin	Function
1	VCON:VC.TCXO NC:TCXO
2	NC
3	NC
4	NC
5	GND
6	CMOS/ Clipped Sinewave Output
7	NC
8	NC
9	Tri-State Control
10	VDD

SOLDER PAD LAYOUT (mm)



ELECTRICAL SPECIFICATION

Parameter	5.0 V		3.3 V		Unit
	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD) 5%	4.75	5.25	3.13	3.47	V
Frequency Range	5	26	5	26	MHz
Standard Frequency (for CMOS)	8.192, 10, 12.8, 20				
Standard Frequency (for Clipped sine)	8.192, 10, 12.8, 16.384, 19.2, 19.44, 20, 25, 26				
Operating Temp. Range	-20 ~ 70 -40 ~ 85				°C
Frequency Stability (Overall, 20 Years)*	–	±4.6	–	±4.6	ppm
Frequency Stability Vs Temp. Range (Ref. to (Fmax+Fmin)/2)	–	±0.28	–	±0.28	ppm
Holdover Stability +	–	±0.37	–	±0.37	ppm
Supply Current (CMOS output)	–	6.0	–	6.0	mA
Supply Current (Clipped Sine Wave)	–	3.5	–	3.5	
Output Level (CMOS)					
Output High (Logic"1")	90%VDD	–	90%VDD	–	V
Output Low (Logic"0")	–	10%VDD	–	10%VDD	
Duty	45	55	45	55	%
Output Level (Clipped Sine Wave)	0.8	–	0.8	–	Vp-p
Load (CMOS)	15pF		15pF		
Load (Clipped Sine Wave)	10 KΩ // 10pF		10 KΩ // 10pF		
Control Voltage Range (VCTCXO)	0.5	2.5	0.5	2.5	V
Pulling Range (VCTCXO)	±5.0	–	±5.0	–	ppm
Vc Input Impedance (VCTCXO)	100	–	100	–	KΩ
Phase Noise @ 12.8 MHz					
100 Hz	-120		-120		dBc / Hz
1 KHz	-140		-140		
10 KHz	-148		-148		
Start Time	–	2	–	2	mSec
Tri-State					
Disable	–	0.3VDD	–	0.3VDD	V
Enable	0.7VDD	–	0.7VDD	–	
Storage Temp. Range	-55	125	-55	125	°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
* Including calibration @ 25 oC , supply voltage VDD±5% , load 15pF±5%, reflow soldering, 20 years aging and frequency stability over temperature.
+ Including 24hours aging , supply voltage VDD±5% and frequency stability over temperature.